FPGAs: Enabling the Software/Reconfigurable Radio

Dr Chris Dick
DSP Chief Architect

Agenda

• Device Technology
• Software
• Design Methodologies
• Example
Why FPGA DSP?

- Flexibility
- High performance
- Time to Market
- Functional extensions to existing equipment
- Standard part (no NRE/Inventory issues)
- Early system bring-up on hardware

The Impact of Moore’s Law

Transistor Count

- RCA - 1962: First MOSFET, Transistors = 4,500
- Intel - 1972: First 8-bit up, Transistors = 4,500
- HP - 1981: 32-bit up, Transistors = 450,000
- Intel Pentium II - 1995: 32-bit up, Transistors = 75M
- Xilinx/UMC Group - 1999: Virtex - 1000, Transistors = 7.4M

Time Period: 1960 to 2000
**Process Drives Density & Performance**

Source: SIA '94, SIA '97, Xilinx

**Virtex-II Platform FPGA**

- **Active Interconnect™**
  - Fully Buffered
  - Fast, Predictable

- **Block RAM**
  - 18KBit True Dual Port
  - Up to 3.5Mbits / device

- **Multipliers**
  - 18b x 18b multiplier
  - 200MHz pipelined

- **Powerful CLB**
  - 8 LUTs
  - 128b distributed RAM
  - Wide Input functions (32:1)
FPGA to ASIC Crossover Improves with Process

ASIC Costs
Start higher, but slope is flatter

For each technology advance, crossover volume moves higher

Problem Today: Integrator’s Dilemma

ASIC SoC
Highly Specialized Point Solution
New Era of Platform FPGAs

- Platform FPGA
- Broad Range of Applications

Applications Space

ASIC
SoC

FPGA Customized Datapaths

- Design tradeoffs and optimization in real (design)-time
Example: FIR Filter

- Use optimum precisions at each node in the computation graph
- ‘Right-size’ the datapath
- design surface for a FIR filter: Area vs Sample Rate vs Length

Adding Parallelism in Conventional DSP Solutions

- New DSP architectures such as VLIW and super-scalar have one goal: provide higher degrees of parallelism
- Architecture evolution along the same design axis is not scalable
  - Too many MAC functional units makes programming, compilers and scheduling an issue
- The effective computing per chip area decreases
  - Memories grow geometrically while the datapath does not
The Power of Parallelism

• In FPGAs we can exploit the large amounts of parallelism inherent in many DSP data paths

FPGAs = Performance (1)

• 12 concurrently operating 64-tap filters
• 8-bit MACs – 8-bit data, 8-bit coefficients†
• Sample Rate (fs) = 154 MHz
• 13,704 slices (95% of device)
• 118 Billion MACs/s
• I/O bandwidth = 237 Giga-bytes/s

† Optimized for coefficient set
FPGAs = Performance (2)

- 1024-point complex FFT
  - 9 microsecond execution time (@fclk = 115 MHz)
  - 2,500† logic slices
- Viterbi decoder at OC3 data rates: 155 Mbps
- Interleaver/de-interleaver @fclk > 200 MHz
- RS decoding @10 Gbps
  - 16 parallel RS decoders in a single XC2V3000-4
**Wideband BTS - Receiver**

- LNA
- LO
- AGC
- ADC
- Mixer channel selection
- Filter + decimation
- Filter + decimation
- Programmable filter

**FPGA front-end signal processor:**
- Channel selection, rate adjust, matched filter, DDS
- Sample rate selection, filter coefficients
- RISC Micro.
- Protocol and control
- Applications/applets
- Rake processor (search, track)
- Adaptive rake
- Demodulator
- FEC: Turbo, Viterbi
- MUD, ICU
- Beam forming

**Building the System**

- Device technology is part of the solution
- The software/IP is getting harder than the hardware
- Design methodologies for
  - Productivity
  - Rapid design exploration
  - Hardware abstraction
  - Single source for all aspects of the design & development cycle
    - Verification
    - Implementation
The Design Space is Rich

- Decision directed T/2 Adaptive Equalizer - LMS based update
- Using FPGAs There are multiple architectural choices available to meet a desired area/performance objective
- Fully parallel
  - N MAC processing elements (PEs)
  - N LMS PEs
- Folded architecture
  - 1 MAC PE & 1 LMS PE for each polyphase segment
- ... Many others
Equalized Receiver Example

Transmitter Model
- 16-QAM Source
- Matched Filter
- Sample rate Change

Passband Adaptive Equalizer
- Fractionally spaced (T/2)
- Polyphase decimator structure
- LMS coefficient update
- coefficients updated at the symbol rate

Carrier Recovery
- CORDIC based PD

System Generator Simulation

TX const.
Transition
diagram

Rx signal
with ISI
& Doppler

Equalized
No carrier lock

Equalized
constellation
Implementation

- Parallel T/2 FSE
- Polyphase decomposition
- 8-taps total
  - 4 taps in each polyphase segment
- 8-LMS PEs
- Coefficients updated at the symbol rate

Pipelined Parallel T/2 DD FSE

- Design components are based on a library of highly optimized module generators

Input sample commutator

Polyphase Filter produces samples at the symbol rate
Pipelined Parallel T/2 FSE

• One polyphase segment
  – 4 FIR PEs & 4 LMS PEs

Pipelined Parallel T/2 FSE

• Design statistics for 8 tap equalizer
  – 2674 logic slices
  – 66 multipliers
    • 64 used for FIR + LMS PEs, 2 for rate adaption
  – fclk = 149.5 MHz (-6 speed grade part)
• Computation rate: 9.6 Giga-MACs

† software version 4.1.03i, speedfile version 1.93, par -rt 5 -pl 5 -xe 2
Folded FSE

- Benchmark data
  - 2093 logic slices
  - 16 embedded multipliers
  - $f_{clk} = 100$ MHz

- For $f_{clk} = 100$ MHz and $N=8$ T/2 FSE the symbol rate is 25 Msym/s
  - For 16-QAM this is 100 Mbps

Carrier Recovery Loop

- Mixer using Virtex-II
- Embedded multipliers: 3 multipliers, 5 additions
- CORDIC based phase detector
- PI Loop filter using 2 embedded multipliers

Look-up table based DDS

Plug Loop filter using 2 embedded multipliers
CORDIC Phase Detector

System Generator Implementation

CRL Resources

<table>
<thead>
<tr>
<th>Function</th>
<th>Slice Count</th>
<th>Block RAMs</th>
<th>Embedded Multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heterodyne</td>
<td>111</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>DDS</td>
<td>5</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>Loop Filter</td>
<td>32</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>Phase Detector</td>
<td>270</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>413†</strong></td>
<td><strong>1</strong></td>
<td><strong>8</strong></td>
</tr>
</tbody>
</table>

† The small slice count discrepancy is due to logic optimizations that occur when the individual CRL components are integrated into the complete system.
DIME - Modular System Building

Board image courtesy of Nallatech http://www.nallatech.com/

The Signal Processing Platform

- Active super-fast interconnect
- Synchronous Dual-Port RAM
- Up to 8 million gates
- Embedded RISC CPU
- Programmable I/Os with LVDS
- 3.125Gb Serial
- XCITE Impedance Control
- Multipliers: 18b x 18b multiplier, 200MHz pipelined
- Embedded RISC CPU
Platform Based Design

• Hardware/Software partitioning

Logic Fabric
Processor

The Future

• Trends
  – Increasing levels of System integration
  – Pervasive DSP enabling anywhere anytime connectivity
  – Increasingly complex systems
  – Decreasing market windows

• FPGA DSP systems
  – Device technology supporting highly parallel DSP engines
  – Design methodologies
    • Abstraction that permits working in the language of the problem
    • Enables effective integration of re-usable components (cores)